REMARKS/ARGUMENTS

Reconsideration and re-examination are hereby requested.

The claims have been provisionally rejected for obviousness double patenting. This issued will be addressed when allowable subject matter is found.

The claims stand rejected under 35 USC 103 as being unpatentable over Martin et al. (U. S. Patent No. 5,214,768) in view of Gaskins (U. S. Patent No. 5,903,911).

The Examiner admits that Martin et al. does not describe a cache memory, a message network operative independently of the data transfer section and wherein the first and second directors control data transfer between the first and second directors in response to messages passing between the first and second directors through the message network as in claims 1-27, 31-45, 49-56. The Examiner also admits that Martin et al. does not describe messages by-passing the data transfer section as in claims 28-30, 46-48, 57, 59, 61-62, 64-65, 67-71, 73-75.

The Examiner points to Gaskins et al, Figures 2, 3 and 4 and column 7, lines 2-34, column 14 lines 4-18 and column 4 lines 39-40 as somehow teaching a message network operative independently of the data transfer section, and points to figure 2 element 208. However, element 208 is a CACHE MEMORY CONTROLLER not a message network operative independently of the data transfer section and wherein the first and second directors control data transfer between the first and second directors in response to messages passing between the first and second directors through the message network as in claims 1-27, 31-45, 49-56. or for providing messages by-passing the data transfer section as in claims 28-30, 46-48, 57, 59, 61-62, 64-65, 67-71, 73-75.

The Examiner seems to be indicating that adding a cache memory to Martin et al, will increase the bandwidth of the Martin et al. system. It is respectfully submitted that by adding a cache memory to the system of Martin et al. will decrease the bandwidth of the Martin et al. system. Applicants recognized that by having an arrangement having a message network for having messages ***by-pass*** the data transfer section or is operative independently of the memory will increase the bandwidth of the system. Applicant's recognition is not described or suggested in either Martin et al. or Gaskins taken either singly or in combination

With regard to the bandwidth teaching in Gaskins, the Examiner points to column 4, lines 30-39. However, reading further, Gaskins points out that:

> In an attempt to increase the bandwidth of the system bus, an alternative prefetch technique may be employed. In this alternative technique, if the microprocessor initiates a write cycle and a cache miss occurs, the word is written directly into an allocated block of the cache memory (rather than into system memory). The cache controller concurrently initiates a burst read request to prefetch and store the remaining words of the block from system memory into the cache memory. Although this technique decreases the duration of signal activity on the system bus (since a write cycle to system memory is unnecessary), an incoherency arises since the word written to cache memory was not updated in system memory. The corresponding block of cache memory must accordingly be marked as "dirty".

Applicant fails to see how this has anything to do with providing an arrangement where messages by-passing the data transfer section or is operative independently of the memory increases the bandwidth of the system.

Clams 58, 60, 63, 66, 72 and 75 point out that the messages passing through the message network have a destination field. The Examiner points to Gaskins at column 7, lines 66-67 presented below:

> The local CPU bus 204 is coupled to an input of comparator 302 for providing a physical address signal from CPU 202. A second input of comparator 302 is coupled to a tag logic circuit 304.

Such does section of Gaskins doe not describe that messages ***passing through the message network*** have a destination field.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

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Date

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